REMARKS/ARGUMENTS

After entry of this amendment, claims 2-10 will remain pending in this application. Claim 1 has been cancelled without prejudice. Claim 2 has been rewritten in independent form, the scope of claim 2 has not been narrowed. Support for the amended claims can be found in the specification, no new matter has been added.

Claims 1-4 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Luz et al. (US Patent 6,321,073) (Luz). Claims 5-6 have been rejected under 35 U.S..C § 103(a) as being unpatentable over US Patent 6,321,073 to Luz et al. in view of Galal et al. (US Patent 6,161,004). (Galal). Claims 7, 8, and 10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent application publication 2002/0114413 A1 to Zarubinsky et al. (Zarubinsky) in view of Galal et al. Claim 9 has been rejected under 35 U.S.C. § 102(e) as being anticipated by Zarubinsky et al. (US Patent application publication 2002/0114413 A1).

Reconsideration of these rejections and allowance of the pending claims in light of these amendments and remarks is respectfully requested.

Claim 2

Claim 2 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Luz. But Luz does not teach each and every element of this claim. For example, claim 2 recites "delay measurement means coupled to the demodulator operable to determine a delay vector characterizing the in-phase and quadrature phase DC components." Luz does not provide this feature.

The pending office action cites column 4, lines 20-38 of Luz as teaching this limitation. (See pending office action, page 3, first paragraph.) But this passage does not teach a delay measurement means as required by the claim. Rather, this passage describes an averaging circuit that averages a number of samples, applicants submit that there is no delay measurement means used in this function.

The delay circuit as claimed provides a circuit that determines the delay vector angle for a portion of a signal path. This angle can then be used to separate I and Q offset

components, which allows their cancellation. (See application, page 7, lines 3-7). Luz does not provide this feature.

For at least these reasons, claim 2 should be allowed.

Claim 5

Claim 5 stands rejected under 35 U.S..C § 103(a) as being unpatentable over Luz in view of Galal. But this combination of references does not show or suggest each and every element of this claim. For example, claim 5 recites: "delay measurement means for determining a delay vector from inputs of the low pass filters to an output of the demodulator." Neither reference provides this limitation.

As before, the pending office action cites Luz, column 4, lines 20-38 as providing this feature. (See pending office action, page 5, section 5.) But this passage refers to an averaging circuit, not a delay circuit.

For at least these reasons, claim 5 should be allowed.

Claim 7

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zarubinsky in view of Galal. But the combination of these references do not show or suggest each and every element of this claim. For example, claim 7 recites "using the first and second quadrature phase components to compute the signal delay." The cited references do not provide this feature.

The pending office action cites Zarubinsky, paragraphs 44 to 82 as show this. (See pending office action, page 8, first partial paragraph.) But Zarubinsky does not compute a signal delay at all, which is logical since the circuitry discussed is for gain control instead of a method of offset correction as claimed.

Delay circuits are provided in the gain control circuit of Zarubinsky in order to synchronize signals. (Zarubinsky, paragraph 47.) Since Zarubinsky is a clocked digital system, these delays can be implement by shift registers. (Zarubinsky, paragraph 77.) Accordingly, there is no need to use the first and second quadrature phase components to compute the signal delay as required by the claim.

Further, applicants submit that the other acts of this method, such as the applying, setting, decreasing, and storing acts are also not shown or suggested by the cited references.

For at least these reasons, claim 7 should be allowed.

Claim 8

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zarubinsky in view of Galal. But the combination of these references do not show or suggest each and every element of this claim. For example, claim 8 recites "determining a signal delay between an output of a second mixer stage of the dual mixer stage radio receiver." The cited references do not provide this feature.

The pending office action cites Zarubinsky, paragraph 77 as showing this limitation. But as discussed above, delay circuits are provided in the gain control circuit of Zarubinsky in order to synchronize signals. (Zarubinsky, paragraph 47.) Since Zarubinsky is a clocked digital system, these delays can be implement by shift registers. (Zarubinsky, paragraph 77.) Accordingly, there is no need to determine a signal delay as required by the claim.

For at least these reasons, claim 8 should be allowed.

Claim 9

Claim 9 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Zarubinsky. But Zarubinsky does not teach each and every element of this claim. For example, claim 9 recites "setting the gain of an automatic gain control to a gain value at which the signal levels of the in-phase and quadrature phase components are less than or equal to the maximum threshold voltage." Zarubinsky does not provide this feature.

The pending office action cites Zarubinsky paragraphs 28, 30, 31, and 89 to 92 as teaching this limitation. (See pending office action, page 4, section 3.) Applicants submit that these sections discuss matching the gains in the I and Q paths as opposed to setting the gain of an automatic gain control to a gain value at which the signal levels of the in-phase and quadrature phase components are less than or equal to the maximum threshold voltage as required by the claim.

For at least these reasons, claim 9 should be allowed.

Other claims

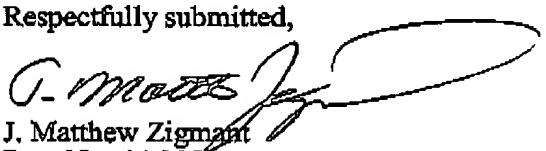
Claim 10 should be allowed for similar reasons as claims 2 and 5. The other claims depend on the above claims, and should be allowed for similar reasons, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,



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